IN THE SPECIFICATION:

Please amend paragraph number **[0002]** as follows:

[0002] State of the Art: Portable electronic devices require data storage, such as a memory device, for providing large storage capacity and low power consumption. To reduce power consumption and extend available power supplies, such as batteries, the memory device typically operates in a low-power mode when stored data is not being accessed. In the low-power mode, supply voltages within the memory device are typically reduced to lower the power consumption of the components. While the supply voltages are varied to reduce power consumption in the ~~low-power~~ low-power mode, data stored within the memory devices must be retained.

Please amend paragraph number **[0026]** as follows:

[0026] Before describing the power reduction circuit 206 in more detail, the various components of the memory device 204 will first be described. The memory controller 202 applies row, column, and bank addresses to an address register 208 over an address bus ADDR. Typically, a row address RA and a bank address BA are initially received by the address register 208 and applied to a row address multiplexer 210 and bank control logic circuit 212, respectively. The row address multiplexer 210 applies either the row address RA received from the address register 208 or a refresh row address RFRA received from the self-refresh counter 246 to a plurality of row address latch and decoder circuits 214A-D. The bank control logic circuit 212 activates the row address latch and decoder circuit 214A-D corresponding to either the received bank address BA or a refresh bank address RFBA from the self-refresh counter 246, and the activated row address latch and decoder circuit latches and decodes the received row address. In response to the decoded row address, the activated row address latch and decoder circuits 214A-D applies various signals to a corresponding memory bank or array 216A-D to activate a row of memory cells corresponding to the decoded row address. The data in the memory cells in the accessed row is stored in sense amplifiers coupled to the array 216A-D, which- also refreshes the accessed memory cells as previously described. The row address multiplexer 210 applies the refresh row address RFRA to the row address latch and

decoder circuits ~~214A-D~~ 214A-D and the bank control logic circuit 212 uses the refresh bank address RFBA when the memory device 204 operates in an auto-refresh or self-refresh mode of operation in response to the memory controller 202 applying an auto- or self-refresh command to the memory device 204.

Please amend paragraph number **[0028]** as follows:

[0028] During data read operations, data being read from the activated array 216A-D is coupled through the I/O gating and data masking circuit 222 to a read latch 224. The I/O gating and data masking circuit 222 supplies N bits of data to the read latch 224, which then applies two N/2 bit words to a multiplexer 226. In a specific embodiment, the I/O gating and data masking circuit 222 may provide 64 bits to the read latch 224 which, in turn, provides two 32 bits words to the multiplexer 226. A data driver circuit 228 sequentially receives the N/2 bit words from the multiplexer 226 and also receives a data strobe signal DQS from a strobe signal generator 230 and a delayed clock signal CLKDEL from a ~~delay-locked~~ delay-locked loop (DLL) circuit 232. The DQS signal has the same frequency as the CLK, CLK* signals, and is used by the controller 202 in latching data from the memory device 204 during read operations. In response to the delayed clock signal CLKDEL, the data driver circuit 228 sequentially outputs the received N/2 bit words as corresponding data words DQ that are in synchronism with rising and falling edges of the CLK signal, respectively, and also outputs the data strobe signal DQS having rising and falling edges in synchronism with rising and falling edges of the CLK signal, respectively. Each data word DQ and the data strobe signal DQS collectively define a data bus DATA coupled to the memory controller 202 which, during read operations, latches each N/2 bit DQ word on the DATA bus responsive to the data strobe signal DQS. As will be appreciated by those of ordinary skill in the art, the CLKDEL signal is a delayed version of the CLK signal, and the DLL circuit 232 adjusts the delay of the CLKDEL signal relative to the CLK signal to ensure that the DQS signal and the DQ words are placed on the DATA bus in synchronism with the

CLK signal. The DATA bus also includes masking signals DQM0-X, which will be described in more detail below with reference to data write operations.

Please amend paragraph number **[0031]** as follows:

[0031] As previously mentioned, in battery-powered electronic devices it is desirable to place the memory device 204 in a standby or low-power mode of operation when the memory controller 202 is not accessing data stored in the memory device. In the memory device 204, exemplary low-power or standby modes include self-refresh and power-down modes. To place the memory device 204 in a self-refresh mode of operation, the memory controller 202 applies a ~~self-refresh~~ self-refresh command to the memory device. In response to the self-refresh command, the command decoder circuit 240 applies control signals to the row address multiplexer 210 and the bank control logic circuit 212 that cause the circuits to utilize the refresh row address RFRA and refresh bank address RFBA from the self-refresh counter 246 to sequentially access each row of memory cells in the memory bank or array 216A-D to thereby refresh the memory cells. The self-refresh counter 246 controls the refresh rate ~~at which~~ of the memory cells in the arrays- 216A-D. The command decoder circuit 240 applies power reduction control signals 300 to power reduction circuit 206 which further reduces power levels within active portions of the memory device 204 by regulating an internal operational power VCCR 302 to portions of the circuitry to a lower voltage level. In other embodiments, other operational powers, an example of which is illustrated as VCCDLL 304, may also be separately regulated to lower operational power levels to isolated components, such as DLL circuit 232, during standby-like modes. The operation of the power reduction circuit 206 during the standby-like modes along with the structure of the power reduction circuit will now be described in more detail.

Please amend paragraph number **[0034]** as follows:

[0034] The power reduction circuit 206′ further includes a switching or routing device for selecting between the first reference signal 308 and the second reference signal 310. By way of example and not limitation, a switching device is illustrated as a multiplexer 312 having inputs for

coupling with at least the first and second reference signals 308, 310, an output for multiplexing one of the inputs therethrough and one or more control inputs for coupling with the power reduction control signals 300 (FIG. 1). In the present embodiment, the power reduction control signals are illustrated as control signals 300′ and are specific to a self-refresh low-power mode causing the selection of a reference signal that causes the operational power level to be reduced during the ~~self-refresh~~ self-refresh mode. The power reduction circuit 206′ further comprises a means for regulating an external power signal to an operational power level consistent with the memory device operational power levels in response to a reference signal 316. In the present embodiment and by way of example and not limitation, the means for regulating the memory device operational voltage is illustrated as a regulator 314 which includes a reference input for coupling with the reference signal 316 at the output of multiplexer 312. The regulator 314 further includes a regulated output which generates operational power VCCR 302. The regulator 314 generates an output from the external operational power VCCX that is proportional to the level of the reference signal 316.

Please amend paragraph number **[0035]** as follows:

[0035] FIG. 2 further illustrates one set of typical voltage levels generated from the illustrated embodiment. As shown, the regulator reference 306 receives an external operational voltage VCCX at a voltage level of 2.5 volts and generates first and second reference signals 308, 310 therefrom. During a nonself-refresh mode of operation, the first reference signal 308 couples to the regulator 314 which regulates an internal operational power VCCR 302 to a level of 2.0 volts. When a self-refresh command is received at the memory device 204 (FIG. 1), the second reference signal 310 couples to the reference input of the regulator 314 and regulates the external operational power VCCX from a level of 2.5 volts down to a level of 1.5 volts. Therefore, when a standby-like command, ~~such as~~ such as a self-refresh command, is received, the memory device 204 (FIG. 1) may isolate and power off certain unnecessary functionality of the memory device 204 with the power reduction circuit 206′ further reducing the power consumed by the memory device 204 by lowering the internal operational power from, for

example, 2.0 volts to 1.5 volts which is within the operational ranges of the remaining functional components of the memory device 204.

Please amend paragraph number **[0041]** as follows:

[0041] FIG. 5 further illustrates one set of typical voltage levels generated from the illustrated embodiment. As shown, the regulator reference 306 receives an external operational voltage VCCX at a voltage level of 2.5 volts and generates first and second reference signals 308, 310 therefrom. During a nonpower-down mode of operation, the first reference signal 308 couples to regulators 314, 318 which regulate an internal operational power VCCR 302 to a level of 2.0 volts and an additional operational power VCCDLL 304 to a level of 2.0 volts. When a ~~power-down~~ power-down command is received at the memory device 204 (FIG. 1), the second reference signal 310 couples to the reference input of regulator 314 and regulates the external operational power VCCX having a level of 2.5 volts to form an internal operational power VCCR 302 having a level of 1.5 volts while retaining operational power VCCDLL 304 having a level of 2.0 volts allowing the DLL to remain in a locked state.